What is claimed is:

1. An information reproducing method that employs a PRML method for comparing a target signal with each reproduced signal for a continuous N time to select the most likelihood one of state changes therein, thereby transforming said reproduced signal to a binary value;

wherein, when said PRML method is represented as PR(α1, a2, ..., αN), the leftmost M1 coefficient and the rightmost M2 coefficient in a coefficient array are all zero while integer values M1 and M2 satisfy a relationship of "M1 ≥ 0, M2 ≥ 0, M1+M2 ≥ 1, M1+M2 < N"; and

wherein, when integer MM = M1+M2 and integer NN = N-MM are satisfied, said method includes:

a step of using a target value obtained by adding 2^N or less compensated values V2 corresponding to a value of an N-bit digital bit array to an initial target level V1 obtained by a convolution operation of each of NN non-zero coefficient values and an NN-bit digital bit array; and

a step of binarizing said reproduced signal to the most likelihood bit array while comparing said reproduced signal with said target value (V1+V2).

2. An information reproducing method that employs a PRML method for selecting the most likelihood one of state changes in a reproduced signal while comparing a target signal with each reproduced signal obtained for a continuous N time, thereby binarizing said reproduced signal to a binary value;

wherein, when said PRML method is represented as PR(α1, a2, ..., αN)ML, the logic of said state change excludes a state change logic of a reproduced signal whose minimum run length is R1 and under in accordance with the minimum run length R1 (R1 ≥ 1);

wherein said method includes:

a step of using a target value obtained by adding 2^N or less compensation values V2 corresponding to a value of an N-bit digital bit array to an initial target level V1 obtained by a convolution operation of each of N coefficient values (α1, a2, ..., αN) and an N-bit digital bit array;

a step of binarizing said reproduced signal to the most likelihood bit array while comparing said reproduced signal with said target value (V1+V2); and

a step of setting a value larger enough than an amplitude of said reproduced signal as said compensation value V2 corresponding to said digital bit array if the run length of said N-bit digital bit array is R2 and under when the minimum run length R2 (R2>R1) signal is to be reproduced.

3. The method according to claim 1,

wherein said method further includes a step of obtaining a compensated reproduced signal by calculating a compensation value V2 for each group of N bits in said binarized bit array, then subtracting the result from said reproduced signal.

4. The method according to claim 3,

wherein a clock used to reproduce information is extracted from said compensated reproduced signal.

5. The method according to claim 1,

wherein a clock used to reproduce information is generated without using phase information obtained from a minimum run length mark.

6. The method according to claim 2,

wherein a clock used to reproduce information is generated without using phase information obtained from a minimum run length mark.

7. An information reproducing drive for outputting a binary value obtained from a reproduced signal with use of a PRML method, said drive comprising:

a PR target output unit for outputting a PR class target value corresponding to an N-bit bit array;

a pattern compensation table for storing a compensation value corresponding to each M-bit (M > N) bit array;

a waveform equalizer for equalizing a reproduced signal; and

a branch metric calculation unit for calculating a branch metric value for each bit array by employing a target value obtained by adding up a PR target value output from said PR target value output unit and a compensation value stored in said pattern compensation table with respect to an output from said waveform equalizer.

8. The drive according to claim 7,

wherein said drive further includes a compensation table study unit for correcting said pattern compensation table so as to minimize an error between an output from said waveform equalizer and said target value calculated in accordance with an obtained binary bit array.

9. The drive according to claim 7,

wherein said drive further includes:

a compensation calculation unit for storing binary class bits and obtaining a compensation value corresponding to said bit array, then subtracting the result from said waveform equalizer; and

a D/A converter for converting an output of said compensation calculation unit to an analog signal.

10. The drive according to claim 9,

wherein said drive further includes a PLL circuit for inputting an output of said D/A converter; and

wherein said PLL circuit generates a clock.